FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5)
1477.011	09/806224

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP99/05942	13 August 1999	29 September 1998

TITLE OF INVENTION

METHOD FOR PRODUCING TRANSISTORS

APPLICANT(S) FOR DO/EO/US

GRUTZEDIEK, Hartmut and SCHEERER, Joachim

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☒ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

This application is entitled to small entity status.

APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/806224	PCT/EP99/05942	1477.011

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1,000.00	
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$860.00	
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$710.00	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00	
	ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**	
	Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	27 - 20 =	7	x $18.00	**$126.00**	
Independent claims	1 - 3 =	0	x $80.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
	TOTAL OF ABOVE CALCULATIONS =			**$986.00**	
	Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**. ☒			**$493.00**	
	SUBTOTAL =			**$493.00**	
	Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +			**$0.00**	
	TOTAL NATIONAL FEE =			**$493.00**	
	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐			**$0.00**	
	TOTAL FEES ENCLOSED =			**$493.00**	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$493.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **08-1935** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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224,778
REGISTRATION NUMBER

March 27, 2001
DATE

BEFORE THE UNITED STATES ELECTED OFFICE

In Re Application of: Grutzediek and Scheerer

Corresponding to International Application No.: PCT/EP99/05942

Filed: 13 August 1999

Title: Method for Producing Transistors

Box PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

Attn: DO/EO/US

PRELIMINARY AMENDMENT

Dear Sir:

For the U.S. national phase, kindly rewrite pending claims 4, 7, 15, 22, 25, and 26 as follows:

4. (Amended) The method of Claim 2, wherein an n-doped junction area having heavier doping than that of the trough is produced in the n-doped fringe area of the trough and a p-doped area having heavier doping than that of the p-doped area enclosed by the p-doped inner area is produced in the p-doped area enclosed by the p-doped inner area.

7. (Amended) The method of Claim 5, wherein in the n-doped fringe area of the trough an n-doped area having heavier doping than that of the trough and in the n-doped area forming the base an n-doped area having heavier doping than that of the n-doped area forming the base and in the p-doped inner area a p-doped area having heavier doping than that of the p-doped inner area are produced.

15. (Amended) The method of Claim 13, wherein an n-doped area having heavier doping than that of the n-doped area forming the gate is inserted into the n-doped area forming the gate.

22. (Amended) The method of Claim 16, wherein n-doped or p-doped areas for the creation of the structures forming the semiconductor components are produced in the active areas.

25. (Amended) The method of Claim 1 employed for the creation of a structure forming a photosensitive transistor in which an n-doped area is implanted into the p-doped inner area, whereby the terminal forming the collector at the fringe area of the n-doped trough and the terminal forming the emitter at the n-doped area implanted into the p-doped inner area is created.

26. (Amended) The method of Claim 1, wherein the p-doped or the n-doped semiconductor substrate is a weakly p-doped or n-doped semiconductor substrate.

REMARKS

By this Preliminary Amendment, multiple dependencies in the pending set of claims have been eliminated to avoid additional costs, and claim 25 has been rewritten in dependent form to provide clear antecedent basis for terminology used in that claim.

Entry of this Amendment and favorable consideration of the application are requested.

Respectfully submitted,

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Dated: March 27, 2001

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Version with markings to show changes made.

4. (Amended) The method of Claim 2 [or 3], wherein an n-doped junction area having heavier doping than that of the trough is produced in the n-doped fringe area of the trough and a p-doped area having heavier doping than that of the p-doped area enclosed by the p-doped inner area is produced in the p-doped area enclosed by the p-doped inner area.

7. (Amended) The method of Claim 5 [or 6], wherein in the n-doped fringe area of the trough an n-doped area having heavier doping than that of the trough and in the n-doped area forming the base an n-doped area having heavier doping than that of the n-doped area forming the base and in the p-doped inner area a p-doped area having heavier doping than that of the p-doped inner area are produced.

15. (Amended) The method of Claim 13[or 14], wherein an n-doped area having heavier doping than that of the n-doped area forming the gate is inserted into the n-doped area forming the gate.

22. (Amended) The method of [one of Claims 16 to 21] Claim 16, wherein n-doped or p-doped areas for the creation of the structures forming the semiconductor components are produced in the active areas.

25. (Amended) [A] The method of Claim 1 employed for the creation of a structure forming a photosensitive transistor in which an n-doped area is implanted into the p-doped inner area, whereby the terminal forming the collector at the fringe area of the n-doped trough and the terminal forming the emitter at the n-doped area implanted into the p-doped inner area is created.

26. (Amended) The method of [one of Claims 1 to 25] Claim 1, wherein the p-doped or the n-doped semiconductor substrate is a weakly p-doped or n-doped semiconductor substrate.

Process for Producing Transistors

The present invention concerns a process for producing integrable transistors.

A number of processes are known in the art for producing pn-junctions in semiconductor components and include diffusion, epitaxy, and ion implantation.

A brief overview of the diverse processes used in producing bipolar transistors is provided in the published article, "Advances in Bipolar VLSI" by George R. Wilson in *Proceedings of the IEEE*, Vol. 78, № 11, 1990, pp. 1707-1719.

In the following, a standard process for producing bipolar transistors is described in detail. Initially, for production of bipolar transistors a subcollector area, also called a buried layer, is diffused into a p-doped semiconductor substrate by which the semiconductor collector series resistance of the transistor can be effectively reduced. Then the semiconductor substrate is coated with an epitactically n-conductive layer. Thereafter electrically isolated areas are partitioned in the epitactic layer. Insulation of these so-called epi-islands is done using the pn-transition layers poled in reverse bias, which are created by deep-diffused p-areas. This is followed by additional diffusion steps with which the base and emitter areas of the NPN-bipolar transistor are defined. Following this, bonding for the transistor terminals is carried out.

In the practice, the standard bipolar process using film insulation has stood the test of time. However, the costly epitaxy and insulation process has been a disadvantage. P-channel field effect transistors with low threshold voltages can be realized using the standard bipolar process only with modifications.

Therefore, the purpose of this invention is to provide a simplified process for producing various types of transistors in a common manufacturing process.

The distinct advantage of the process described in the invention is that an epitaxy and insulation process as used in the standard bipolar process is no longer necessary.

In the process described in the invention an n-doped trough is produced by high-energy implantation in the preferably weakly p-doped semiconductor substrate. The ion implantation is done using an energy that assures that a p-doped inner area remains on the surface of the semiconductor substrate, while the fringe area of the n-doped trough extends as far as the surface of the semiconductor substrate.

It is also possible to carry out ion implantation using an energy that is not sufficiently high as to leave a p-doped inner area at the surface of the semiconductor substrate, but produces a weakly n-doped inner area. In this instance the p-doped inner area is produced in that the back-scattered ions are compensated using p-doped materials. Said compensation can be done using ion implantation or diffusion with or, over larger areas, without the use of a mask.

Alternatively an n-doped semiconductor substrate can be used as the basis. In this instance all implant ions are replaced by a complementary species; that is, n-implant ions are substituted for p-implant ions and *vice versa*. The semiconductor substrate is preferably a weakly p-doped or n-doped semiconductor substrate.

On the basis of the semiconductor structure described in the foregoing both NPN-transistors and PNP-transistors can be manufactured in the most various embodiments. To achieve this, additional n-doped and/or p-doped areas forming the transistor structure are inserted into the p-doped inner area of the semiconductor substrate.

In order to produce the n-doped trough, a mask is applied to the semiconductor substrate and defines a window that is bordered by a peripheral edge. Independent of the formation of the edge of the window, a deep n-doped trough is inserted into the semiconductor substrate using ion implantation. The fringe area of the trough extends as far as the surface of the semiconductor substrate. The formation of the fringe zone that extends as far as the surface of the semiconductor substrate is explained by the fact that the ions are slowed at different rates at a vertical edge and at a slanted edge.

On the basis of the semiconductor structure described in the foregoing, an NPN-transistor can be produced simply and without great cost in that a p-doped area with heavier doping that that of the semiconductor substrate is produced in the p-doped inner area of the semiconductor substrate. Said p-doped area with the heavier doping then forms the base of the transistor. A preferable highly n-doped area that is inserted into the p-doped area then forms the emitter of the transistor. Since the fringe area of the n-doped trough that serves in this instance as the collector reaches as far as the surface of the semiconductor substrate, the collector connection via the strongly n-doped area can be easily made in this semiconductor structure.

In order to create a semiconductor structure for a PNP-transistor, an n-doped area is created in the p-doped inner area. Said area forms the basis of the transistor. In the n-

doped area enclosed by the p-doped inner area a preferably highly p-doped area forming the emitter of the transistor is created. The p-doped inner area then forms the collector of the transistor.

The production of the n-doped and/or p-doped area in the semiconductor substrate can be accomplished using process steps known to those skilled in the art. It is advantageous if the shallow areas; i.e., those close to the surface are produced by ion implantation.

The areas in which ions are to be implanted can be defined using conventional masking processes. The masking material can consist of a photoresist, metal, glass or other material. Preferably the structure of the areas to be doped and defined using masks is marked using lithographic methods. Also possible are combinations of lithography and etching methods.

For the ohmic contact of the transistor terminals, additional n-doped and/or p-doped junction areas with a heavier doping can be inserted into the semiconductor structure.

An NPN-transistor can also be created in that an n-doped area is produced in the p-doped inner area which forms the emitter of the transistor. In this embodiment, the p-doped inner area then forms the base and the n-doped trough forms the collector of the transistor. It has been shown that this NPN-transistor demonstrates high gain.

On the basis of the semiconductor structure with the elevated trough described in the foregoing, I^2L (Integrated Injection Logic) or field effect transistors can be produced inexpensively.

Furthermore, on the basis of said semiconductor structure, also logic gates with high packing density can be produced. To achieve this, the active regions of the logic gate must be partitioned in the semiconductor structure. The semiconductor structure using the elevated trough also allows photosensitive diodes and transistors to be produced inexpensively.

The separation can be done by ion implantation using a supplemental mask. When done in this manner, the area of the trough covered by the mask is drawn upwards. Over said elevated trough area either an n-doped area or an oxide layer extending as far as the trough is produced in the p-doped inner area. Instead of the coverage by the mask the trough can be elevated also using local oxidation that is done prior. Alternatively, the separation of the active areas can be done also using n-doped areas which extend into

the trough. A further possibility for separation is done by providing the semiconductor substrate with slots or incisions that extend into the trough (trench insulation).

In the following, several illustrative embodiments of the process for producing transistors or logic gates are described by detailed reference to the accompanying drawings, wherein:

Figures 1a to 1c depict the step in production of an n-doped trough in the semiconductor substrate using high energy ion implantation, whereby the mask defining the window for ion implantation is delimited by an edge running perpendicular or tilted inward or outward;

Figures 2a to 2d depict the further process steps for producing an NPN-transistor starting with the semiconductor structure depicted in Figures 1a to 1c;

Figures 3a to 3d depict the further process steps for producing a PNP-transistor starting with the semiconductor structure depicted in Figures 1a to 1c;

Figures 4a to 4e depict the further process steps for producing an alternative embodiment of an NPN-transistor that is characterized by a high gain and based on the semiconductor structure depicted in Figures 1a to 1c;

Figures 5a to 5d depict the individual process steps for producing an I^2L (Integrated Injection Logic) element, starting with the semiconductor structure depicted in Figures 1a to 1c;

Figures 6a to 6e depict the individual process steps for producing a field effect transistor starting with the semiconductor structure depicted in Figures 1a to 1 c, and

Figures 7a to 7f depict the individual process steps for producing a logic gate with implanted insulation;

Figures 8a to 8e depict the individual process steps for producing a logic gate with low-frequency modulated trough and implanted insulation;

Figures 9 a to 9e depict the individual process steps for producing a logic gate with low-frequency modulated trough and oxide insulation;

Figures 10a to 10f depict the individual process steps for producing a logic gate with trench insulation, and

Figures 11a to 11d depict the individual process steps for producing photosensitive diodes;

Figures 12a to 12c depict the individual process steps for producing an initial illustrative embodiment of a photosensitive transistor with open base;

Figures 13a to 13d depict the individual process steps for producing a photosensitive transistor with enhanced photosensitivity;

Figures 14a to 14d depict the individual process steps for producing a photosensitive transistor with enhanced withstand voltage;

Figures 15a to 15f depict the individual process steps for producing a lateral PNP-transistor.

The semiconductor structure described with reference to Figures 1a to 1c is the prerequisite for production of the various semiconductor components. In the following, the individual process steps for producing said semiconductor structure are described.

A mask 2 is applied to a weakly p-doped semiconductor substrate 1 (wafer); said mask exhibits a window 3 that is delimited by a peripheral edge 4. A wafer made of a weakly p-doped monocrystalline silicon with a resistance of from, for example, 5 Ohms cm is used as the preferred basic material. Other suitable semiconductor materials are, for example, GaAs and SiC together with the doping agents appropriate for these materials. The mask material can be a photoresist, metal, glass or even another material. Preferably the structure is created by a photolithographic process.

The formation of the edge 4 of the mask window 3 is irrelevant to the further process steps. The edge 4 of the mask window 3 can be formed vertically (Figure 1a), slanted outward (Figure 1b) or slanted inward (Figure 1c).

Following creation of the mask, which can be done using conventional processes, doping is done, preferably an implantation of phosphorus ions at a dose of, for example, 2×10^{13} atoms/cm^2, in order to create an n-doped trough 5 in the semiconductor substrate 1. The implantation energy in this process is such that over the trough 5 in the semiconductor substrate 1 there still remains a p-doped area 6. At a dose of 2×10^{13} atoms/cm^2 this is, despite the back-scattered phosphorus ions, for example, the case if the implantation energy is 6 MeV phosphorous ions.

With high-energy implantation there is a peculiar effect in the area of the edge 4 of the mask window 3. Since the ions are scattered at the vertical edge or are slowed down at different intensities at the slanted edges, a fringe area 7 forms extending upwards in the trough 5, said area extending as far as the surface of the semiconductor substrate 1 and encloses the remaining p-doped area 6 at the surface of the semiconductor substrate.

To produce an integrated circuit and by using an appropriate mask, a number of n-doped troughs, whose fringe areas extend to the semiconductor substrate surface, can be inserted using ion implantation.

Alternatively, however, ion implantation can also be done using an energy that is sufficient to cause a p-doped inner area to remain at the surface of the semiconductor substrate. For example, at an implantation energy of 2 MeV and a dose of 2×10^{13} atoms/cm^2, the back-scattered phosphorus ions reach the surface of the wafer in sufficient number and no weakly p-doped area remains but an n-doped semiconductor with a concentration of $N_p > 10^{15}/cm^{-3}$ does. This is prevented in that either a wafer with an overall higher p-concentration is used as the starting material or additional doping is inserted into the wafer surface for the purpose of compensation. This can be done by implantation or diffusion. For example, compensation can be produced with an implantation energy of 200 KeV and a dose of 3×10^{11} atoms/cm^2 to a depth of 8 µ. However, these are merely reference values that can be changed multiply. The re-doping can be done over the entire surface or only within the trough using a mask.

Starting with the semiconductor structure described with reference to Figures 1a to 1c various transistor types can be produced.

Figures 2a to 2d illustrate the steps for producing an NPN-transistor. In the p-doped inner area 6 of the semiconductor structure (Figure 2a) enclosed by the n-doped trough of Figures 1a to 1c, a central rectangular, round or other shaped p-doped area 8 is inserted using ion implantation and using conventional doping ($N_A = 10^{18}$ cm^{-3}) which is heavier than that of the semiconductor substrate (Figure 2b). Then, using ion implantation, a shallow peripheral n^+-junction area 9 having the conventional doping concentration ($N_D \sim 10^{22}$ cm^{-3}) in the fringe area 7 of the trough 5 and a shallow n^+-doped area 10 ($N_D = 10^{22}$ cm^{-3}) is inserted in the p-doped area 8 enclosed by the inner area 6 (Figure 2c). In a further implantation step a shallow p^+-doped junction area 11 ($N_D = 10^{22}$ cm^{-3}) is inserted into the p-doped area 8 (Figure 2d). Finally, the insulation area (not shown) can be constructed and the bonding of the transistor connectors to the n^+ or

the p^+ junction areas can be done using the conventional processes (*vide supra*: G.R. Wilson). In this illustrative embodiment the n-doped trough 5 forms the collector C, the p-doped inner area 6 together with the p-doped area 8, the base B, and the n^+-doped area 10 forms the emitter of the NPN-transistor.

Production of a PNP-transistor likewise starts with the semiconductor structure depicted in Figures 1a to 1c. Using ion implantation, a central n-doped area 12 ($N_D = 10^{18}$ cm^{-3}) is inserted (Figure 3b) into the p-doped inner area 6 (Figure 3a). Then, using ion implantation, a peripheral shallow n^+-junction area 13 ($N_D = 10^{22}$ cm^{-3}) is inserted into the fringe area 7 of the trough 5 and a shallow, lateral n^+-junction area 14 ($N_D = 10^{22}$ cm^{-3}) is inserted into the central n-area 12 (Figure 3c). Then, in a further process step, a peripheral shallow p^+-junction area ($N_D = 10^{22}$ cm^{-3}) is inserted into the inner area 6 and a lateral shallow p^+-area 16 ($N_D=10^{22}cm^{-3}$) is inserted into the central n-area 12 using ion implantation. The p-inner area 6 now forms the collector C, the central n-area 12 the base B and the p^+-area 16 the emitter E of the PNP-transistor, whereby the highly-doped junction areas are provided for producing an ohmic connection to the transistor terminals (Figure 3d). The bonding of the transistor terminals can be done using conventional processes. In order to increase the turnover/breakdown voltage between emitter and collector, in practical applications base and trough can be electrically connected to one another.

Figures 4a to 4d depict the process steps for producing a further embodiment of an NPN-transistor that is characterized by a high gain (super-beta-transistor). Starting with the semiconductor structure (Figure 4a) of Figures 1a to 1c, an n-doped area 17 ($N_D = 10^{18}$ cm^{-3}) is produced in the inner area 6 by means of ion implantation (Figure 4b). Then, using ion implantation, a peripheral shallow n^+-junction area 18 ($N_D = 10^{22}$ cm^{-3}) in the fringe area 7 of the trough 5 and a shallow n^+-junction area 19 ($N_D = 10^{22}$ cm^{-3}) in the n-area 17 are produced by means of ion implantation (Figure 4c). Thereafter a shallow p^+-junction area 20 ($N_D = 10^{22}$ cm^{-3}) is produced in the inner area 6 using ion implantation. The trough 5 now forms the collector C, the inner area 6 the base B, and the n-area 17 the emitter E of the super-beta-NPN-transistor. At the junction areas 18, 19, and 20 bonding of the transistor terminals is again done. In the above embodiment of the invention, the stack consisting of the n-doped area 17 and the n^+-doped area 19 are not unconditionally required; in principal, the n^+-doped area 19 is sufficient. The stack, however, reduces the risk of metallic shorting, whereby the efficacy is improved. The n^+-

doped area 19 does not even have to lie within the n-doped area 17. Areas 17 and 19 can also overlay or only partially overlap each other.

Figure 4e depicts a partial view of the embodiment as described in Figures 4a to 4d, in which the n^+-doped area 19 and the n-doped area 17 overlay each other without area 19 being enclosed by area 17.

Figures 5a to 5d depict the process steps for producing an I^2L element starting with Figures 1a to 1c. Initially n-doped areas, for example four n-doped areas 21, 22, 23, 24 ($N_D=10^{18}cm^{-3}$) are inserted into the inner area 6 by means of ion implantation. Area 21 extends from the fringe area 7 of the trough 5 into the fringe region of the inner area 6 (Figure 5b). In the next process step, a peripheral shallow n^+- junction area 25 ($N_D\sim10^{22}cm^{-3}$) in the fringe area 7 of the trough 5 and in the n-doped areas 22, 23, 24 further shallow n^+-junction areas 26, 27, 28 ($N_D=10^{18}cm^{-3}$) are produced using ion implantation. In the n-area 21 that connects the fringe area 7 of the trough 5 with the inner area 6 a shallow p^+-doped area 29 ($N_D=10^{22}cm^{-3}$) is produced. A further p^+-junction area 30 ($N_D=10^{22}cm^{-3}$) is inserted into the inner area laterally adjacent to the n^+-junction areas 26, 27, 28. The inner area 6 then forms the base of a multi-collector transistor, while the n-areas 22, 23, 24 form the individual collectors C1, C2, C3 of the inversely operated transistor. The injector terminal INJ is created at the p+ area 29 and the terminal of the base B at the junction area 30 and the collectors C1, C2, C3 at the junction areas 26, 27, 28 using conventional bonding processes.

The feed of the supply current into the I^2L element via an injector PNP is only a preferred version. Even a high-ohm resistance or a current source / power supply are conceivable.

Figures 6a to 6d depict the process steps for producing a field effect transistor which is characterized by high turnover/breakdown voltage and slope. Fabrication is based on Figures 1a to 1c (Figure 6a). Using ion implantation, a rectangular n-doped area 31 is inserted into the p-doped inner area 6 of the trough 5; said rectangular n-doped area extends over the entire width, but not over the entire length of the inner area 6, such that the inner area is separated into two regions (Figure 6b). Then, using ion implantation, a peripheral shallow n+ junction area 32 ($N_D=10^{22}cm^{-3}$) is inserted into the fringe area 7 of the trough 5 and a shallow n+ junction area 33 ($N_D=10^{22}cm^{-3}$) is inserted into the n-area 31. Said areas form the gate of the transistor (Figure 6c). Then, in each of the two regions of the inner area 6 one p^+-doped area 34 ($N_D=10^{22}cm^{-3}$) is produced. The p^+-

doped implants 34 represent the junction areas for metal bonding of drain and source of the transistor (Figure 6d). Figure 6e depicts the field effect transistor viewed from above.

The method for producing the various transistor types is advantageous inasmuch as the costly epitaxy and insulation steps are eliminated. All transistor types can be produced starting with the same semiconductor structure using the described process steps simultaneously in a common production process. The individual process steps for producing the n-doped or p-doped areas in the semiconductor structure can also be done in a sequence other than that described in the above illustrative embodiments. Generally, arsenic or phosphorus ions with an energy of 5 to 50 keV are used for n+ implant ions. The energies for the n-implant ions are correspondingly higher at 30 to 100 keV. In p- and p+ implant ions generally boron ions are used with comparable energies as in the n- and n+ implant ions. The indicated concentrations and energies are values used in practice and can be increased or decreased. Other methods for introducing the doping are also possible. Interruptions of the doped areas are likewise possible. n and n^+ or p and p+ as stacks with or without overlap are not absolutely necessary; n+ or p^+ are sufficient. If, however, an n and a p implant ion are below, this arrangement reduces the risk of metal shorting by the n+ or p+ layers and consequently improves efficacies and can change the electrical data of the components. With the base terminal and drain/source n or p can be underlying. Therein the masking can be done using the photolithographic processes in the practice.

In order to make possible a particularly low-impedance bulk resistor it is advantageous if the junction area in the fringe area of the n-doped trough is not designed as a shallow area but as an area that extends deeper into the semiconductor substrate. Thus, the junction area can, for example, extend to a depth at which the n-doped trough lies. However, to achieve this an additional process step is required.

The geometric arrangement of collector, emitter, and base in the trough is depicted in the illustrations for exemplar purposes only. Both size and length can be changed. Structures described as rectangles can have also other shapes; for example, round shapes.

Along with the components described above, further logic gate types can be produced in a common production process starting with the semiconductor structure described with reference to Figures 1a to 1c. Figures 7 to 10 depict the individual steps of various methods for producing logic gates, which are based on said semiconductor structure,

whereby the masks and areas corresponding to each other are identified with the same reference symbols.

Figure 7a depicts the step for producing the n-doped trough 5 in the semiconductor substrate 1 by means of high-energy implantation. The mask 2 with the window 3 is applied to the semiconductor substrate such that during implantation the elevated fringe area 7 is formed in the trough 5 and extends as far as the surface of the semiconductor substrate and encloses the remaining p-doped inner area 6 at the surface of the semiconductor substrate (compare with Figures 1a to 1c).

Then the active regions of the logic gate are separated in the semiconductor substrate in which further n-doped and/or p-doped areas are inserted for the purpose of forming the logic gate. For separation, using ion implantation, an n-doped separation area 35 is produced, which extends into the n-doped trough, surrounding the active region in the inner area 6 of the semiconductor substrate. The implantation is done after application of a mask 36 using conventional processes. With said implanted insulation a number of regions can be separated in the semiconductor substrate which lie densely alongside each other, in order to achieve a high packing density. The further steps in producing a logic gate in one of these regions is described in the following.

After application of an additional mask 37, for example, a rectangular n-doped area 38 and a, for example, rectangular n-doped area 39 are produced in the p-doped inner area 6, whereby areas 38, 39 extend beyond the separation area 35 or lie within the separation area 35. Between the n-doped areas 38, 39 two, for example rectangular, n-doped areas 40, 41 are inserted alongside one another into the p-doped area 6. The creation of the n-doped areas 38 to 41 is done by means of ion implantation using the conventional method (Figure 7c).

After application of a further mask 42 in the external n-doped area 38, a shallow n^+-doped junction area 43 is produced for the terminals of the logic gate, while within the external n-doped area 39 a shallow n^+-doped junction area 44 is produced. In the inner n-doped areas 40, 41 similar shallow n^+-doped junction areas 45, 46 are created (Figure 7d).

Thereupon, a further mask 47 is applied in order to produce a shallow p^+-doped junction area 48 in the internally situated region of the outer n-doped area 38 and a shallow p^+-

doped junction area 49 in the inner area 6 between the internal n-doped area 41 and the external n-doped area 39 (Figure 7e).

An insulation layer 50 is applied to the semiconductor structure and is exposed in the region of the terminals. The trough terminal W is made at the external n^+-doped junction areas 43, 44; the terminal of the injector Inj. for the supply current at the p^+-doped junction area 48, which lies within the external n-doped area 38, the gate terminals C_1, C_2 at the inside n^+-doped junction areas 45, 46 and the terminal B for control of the gate at the p^+-doped junction area 49 (Figure 7f).

In the logic gate described with reference to Figure 7 the active area is separated by an implanted separation area. Figure 8 depicts a method in which an additional implantation is not required for separation of the active area. The method according to Figure 8 differs from the method according to Figure 7 in that the creation of the starting structure by high-energy implantation is done by using an additional mask. The individual masks and areas in Figure 8 that correspond to those of Figure 7 are keyed using the identical reference identifiers.

Figure 8a depicts the starting structure which, with the exception of the use of the additional mask, is produced using the method described with reference to Figures 1a to 1c. Prior to ion implantation a second mask 51, which encloses the region to be separated, is applied in a second lithography step onto the semiconductor substrate within the window 3 of the mask 2. The second mask 51 has a lesser thickness than that of the first mask; it is approximately half as thick.

After placement of the mask, doping is carried out, preferably implantation of phosphorus ions using a dose of, for example, 2×10^{13} ions/cm^2, in order to create the n-doped trough 5 in the semiconductor substrate. In said process the region of the trough 5 covered by the second mask 51 is drawn upward. Then the n-doped areas 38, 39, 40, 41 in the p-doped inner area 6 are produced, whereby the outlying n-doped areas 38, 39 extend as far as the elevated region of the trough 5 (Figure 8b). The process step according to Figure 8b corresponds to the step according to Figure 7c. The separation of the active area by the trough 5 drawn upward in conjunction with the externally situated n-doped areas 38, 39 makes possible an even higher packing density.

Two further doping steps follow and correspond to those of Figures 7d to 7f. At all events a further opening 51 is exposed in the mask 42' over the elevated fringe area 7 of the

trough 5, in order to create a further n^+-doped junction area 52 that serves in the connection of the trough (Figure 8c). The insulation layer 50' over the n^+-doped junction area 43 or 53 is exposed for the trough connection (Figure 8e).

The process described with reference to Figure 9 starts with the semiconductor structure which is produced in the steps as in the case of the semiconductor substrate pursuant to Figure 8a. However, for the separation of the active region, an oxide layer 53, 54 is applied, which extends as far as the trough, in lieu of the n-doping above the elevated region of the trough 5 (Figure 9a). Thereupon further doping steps follow, with the exception of those of Figures 8b to 8e, in that the doping above the elevated area of the trough 5 are eliminated and the outlying n-doped area 38' and the n^+-doped junction area 43' merely approximate or extend only minimally into the oxide layer 53, but not over the elevated region of the trough 5. The modified masks are identified with the references 42'', 47'. In order to create a terminal for the base of the injector Inj. the insulation layer 50'' is exposed above the junction area 43' (Figure 9e). Otherwise the terminals are provided as in the logic gate according to Figure 8.

Figures 10a to 10f depict the individual process steps for producing a logic gate in which the active area is separated by trenches. The process again starts with a semiconductor substrate with an elevated trough 5 (Figures 1a to 1c). In the p-doped inner area 6 n-doped areas 38, 40, 41 are again produced after application of mask 37 (Figure 10b). After application of an additional mask 42'' n^+-doped junction areas 43, 45, 46, 55 are produced (Figure 10c) in areas 38, 40, 31 and in the region of the elevated edge 7 of the trough 5. Thereupon, after application of a further mask 47, a p^+-doped area 49 is created in the inner area 6 and a p^+-doped area 48 is created in the internal region of the external n-doped area 38 (Figure 10d). At this point separation of the active region is done by two trenches 56, 57 extending into the trough 5 lateral to the p^+-doped area 49 and the n-doped area 38 (Figure 10e). The trenches are then re-filled using the conventional method. Figure 10f depicts the semiconductor substrate covered with the insulation layer 50'' with the terminals for the logic gate.

The individual doping steps for producing the logic gate can be carried out in various sequences. Thus, for example, it is not absolutely necessary to carry out the process steps for separation of the active areas of the logic gate before the doping steps for producing the logic gate. Moreover, the individual doping steps can initially be done and the active regions of the logic gate separated later using the method described above.

Semiconductor structures other than those described above can be produced by using the basic structure and separating individual regions.

The dimensions of the overlap of the various dopings are the result of following the conventional rules of production. Double implantation of the same species at one site with n^+ over n or p^+ over p can then be eliminated at said site if a terminal surface is not required or a pn junction already exists with an implantation.

Implantation can be done according to the conventional rules through the window of the insulator (autoregulation) or several implantations can be done through the same mask. The separation of the doping is done by diffusion or oblique implantation. Other methods familiar to the specialist for production of the PN junctions and terminals can also be reasonably used as, for example, dopings comprised of a poly Si layer.

Figures 11a to 11d depict the individual process steps for producing photosensitive diodes on the basis of the semiconductor structure described with reference to Figures 1a to 1c. For the purpose of bonding the n-doped trough 5, after application of a mask 58 in the fringe area 7 of the inner area 5 reaching to the surface of the semiconductor substrate 1 a peripheral, shallow n^+-doped junction area 59 is implanted (Figure 11b). The bonding of the p-doped inner area 6 is done with a shallow p^+-doped junction area 60, which, after application of a mask 61, is implanted in the inner area 6. At the same time a further shallow p^+ junction area is implanted outside of the trough 5 in the semiconductor substrate 1 (Figure 11c). Then a translucent insulation layer 63 is applied onto the semiconductor substrate 1 which is exposed in the regions of the junction areas 59, 60, 62. At the exposed regions of the insulation layer 63 bonding is established with contacts/terminals 1 to 3. Thus two PN junctions are created. The terminals of the first photosensitive diode form contacts 1 and 2, while contacts 2 and 3 form the terminals for the second photosensitive diode. Because of the varying depth of the PN junctions, both diodes are disposed of a high spectral sensitivity at various wavelengths. The first diode is sensitive for short-wave light and the second diode is for long-wave light. Based on the semiconductor structure according to Figures 1a to 1c, however, only one of the two diodes can be produced.

In the following, various methods for producing photosensitive transistors with open base are made clear based on the semiconductor substrate described with reference to Figures 1a to 1c.

After application of a mask 64 a peripherally oriented, shallow n^+-doped junction area 65 is implanted, as in the manufacture of the diodes (Figures 11a to 11d), in the elevated fringe area 7 of the n-doped trough 5. An n^+-doped area 66 is implanted in the p^--doped inner area 6 (Figure 12b). Thereupon a translucent insulation layer 67 is applied onto the semiconductor substrate which is exposed in the region of the n^+-doped junction area 65 as well as in n^+-doped area 66. Bonding of the terminals for the emitter E and collector C is done in the exposed regions of the insulation area 67.

The photosensitivity of the phototransistor according to Figures 12a to 12c can be increased by additional implantation with n-doped material. Figures 13a to 13d depict the individual process steps for producing a photosensitive transistor with increased photosensitivity on the basis of the semiconductor structure according to Figures 1a to 1c. After application of a mask 68 a peripheral n-doped area 69 is implanted in the elevated fringe area 7 of the n-doped trough 5. At the same time an n-doped area 70 is implanted in the p^--doped inner area 6 (Figure 13b). Thereupon a shallow n^+-doped junction area 71 is implanted in the peripheral n-doped area 69. An n^+-doped area 72 is similarly implanted in the central n-doped area 70. The implantations are done after application of a mask 73 (Figure 13c). Thereupon a translucent insulation layer 74 is applied that is exposed over the n^+-doped junction area 71 and the n^+-doped area 72. At the exposed sites the bonding of the emitter E and the collector C is again carried out (Figure 13d).

A photosensitive transistor with increased withhold voltage, but reduced photosensitivity can be created by additional implantation with p-doped material. Figures 14a to 14d depict the individual production steps of such a phototransistor. The production process differs from the process described with reference to Figures 13a to 13d in that after application of a mask 76 it is not an n-doped but a p-doped area 74 that is implanted in the p^--doped inner area 6 (Figure 14b). In the elevated fringe area 7 of the n-doped trough 5 a shallow n^+-doped junction area 77 and a further n^+-doped junction area 78 is then implanted in the p-doped area 75. The implantation is again done after application of a mask 79 (Figure 14c). A translucent insulation layer 80 which is exposed over the n^+-doped junction area 77 and the n^+-doped junction area 78 for the terminals of the emitter E and the collector C, covers the semiconductor substrate (Figure 14d).

Starting with the semiconductor structure described with reference to Figures 1a to 1c a lateral PNP-transistor can be produced as described below.

Figure 15a depicts the step for producing the n-doped trough 5 in the semiconductor substrate 1 by means of high-energy implantation. The mask 2 with the window 3 is applied to the semiconductor substrate so that during the ion implantation the elevated fringe area 7 forms in the trough 5; said fringe area extends as far as the surface of the semiconductor substrate and the remaining p^--doped inner area 6 and wraps around at the surface of the semiconductor substrate.

A further high-energy ion implantation in the inner area 6 using a mask with n-doping and a dose of approximately 1 x $10^{13}/cm^2$ is done in a manner similar to that depicted in Figure 1a to 1c. A trough 5' is formed in the trough 5 with a residual p^--inner area 6' and an elevated fringe 7' as far as the surface of the substrate (Figure 15b).

After application of the mask 81 shallow n^+-terminal dopings are implanted in the peripheral areas 85 and 86 (Figure 15c). Mask 82 defines the region 87 and 88 within the trough 5 and region 89 within the trough 5' (Figure 15d). Said implantation can also be omitted. Mask 83 defines the shallow p^+-terminal implantation in the areas 90 and 91 (Figure 15e).

The regions 85 and 86 freed of the insulation 84 are the base terminals, regions 90 and 91 are the collector terminals, region 92 is the emitter terminal of the PNP. The elevated fringe 7' of the trough 5' forms the base of the lateral PNPs. The trough 5 with the elevated fringe 7 serves as insulation and can be used as a base terminal as can the elevated fringe 7' of the trough 5'. The gain of the transistor can be set by the implant ion dosage of trough 5'.

Patent Claims

1. A method for producing integrable semiconductor components, in particular transistors, diodes, and logic gates, starting with a p-doped or n-doped semiconductor substrate in the following steps:

   application of a mask onto the semiconductor substrate for definition of a window delimited by a peripheral edge;

   production of an n-doped trough in the p-doped semiconductor substrate or p-doped trough in the n-doped semiconductor substrate by means of ion implantation through the mask using an energy that will assure that a p-doped or an n-doped inner area remains on the surface of the semiconductor substrate, whereby the fringe area of the n-doped or p-doped trough extends up to the surface of the semiconductor substrate or creation of an n-doped or p-doped area that extends up to the surface of the semiconductor substrate by using ion implantation through the mask, whereby p-doping or n-doping is inserted into the n-doped area or into the p-doped area such that a p-doped or n-doped inner area is created in the n-doped area or in the p-doped area and is enclosed by the n-doped or p-doped area;

   production of additional n-doped and/or p-doped areas in the p-doped or n-doped inner area and in the fringe are of the n-doped or the p-doped trough that form the structure of the semiconductor component.

2. The method of Claim 1 wherein, for creation of the structure forming an NPN-transistor, a p-doped area having heavier doping than that of the semiconductor substrate together with the p-doped area enclosed by the p-doped inner area forming the base of the transistor and an n-doped area forming the emitter of the transistor are produced in the p-doped inner area, whereby the n-doped trough forms the collector of the transistor.

3. The method of Claim 2, wherein the n-doped area forming the emitter has heavier doping than that of the n-doped trough.

4. The method of Claim 2 or 3, wherein an n-doped junction area having heavier doping than that of the trough is produced in the n-doped fringe area of the trough and a p-doped area having heavier doping that that of the p-doped area

enclosed by the p-doped inner area is produced in the p-doped area enclosed by the p-doped inner area.

5. The method of Claim 1, wherein for the creation of a structure forming a PNP-transistor an n-doped area enclosed by the p-doped inner area is produced in the p-doped inner area and forms the base of the transistor and in the n-doped area a p-doped area forming the emitter of the transistor is produced, whereby the p-doped inner area forms the collector of the transistor.

6. The method of Claim 5, wherein the p-doped area forming the emitter of the transistor has heavier doping that that of the semiconductor substrate.

7. The method of Claim 5 or 6, wherein in the n-doped fringe area of the trough an n-doped area having heavier doping than that of the trough and in the n-doped area forming the base an n-doped area having heavier doping than that of the n-doped area forming the base and in the p-doped inner area a p-doped area having heavier doping than that of the p-doped inner area are produced.

8. The method of Claim 1, wherein for the creation of the structure forming an NPN-transistor having high gain in the p-doped inner area an n-doped area forming the emitter of the transistor is produced, whereby the p-doped inner area forms the base and the n-doped trough forms the collector of the transistor.

9. The method of Claim 8, wherein an n-doped area having heavier doping than that of the trough and in the n-doped area forming the emitter an n-doped area having heavier doping than that of the area forming the emitter and in the p-doped inner area a p-doped area having heavier doping than that of the p-doped inner area are produced in the fringe area of the n-doped trough.

10. The method of Claim 1, wherein an n-doped area joining the fringe area of the n-doped trough with the p-doped inner area and in the p-doped inner area at least one n-doped area are produced for the creation of the structure forming an I^2L element, whereby the p-doped inner area forms the base of a multi-collector transistor and at least one n-doped area enclosed by the p-doped inner area forms the individual collectors of the transistor.

11. The method of Claim 10, wherein in the n-doped area joining the fringe area of the n-doped trough with the p-doped inner area a p-doped area is inserted

12. The method of Claim 11, wherein a p-doped area having heavier doping than that of the semiconductor substrate and in the at least one n-doped area enclosed by the p-doped inner area an n-doped area having heavier doping than that of the n-doped area are produced in the p-doped inner area.

13. The method of Claim 1, wherein for the creation of a structure forming a field effect transistor an n-doped area forming the gate of the transistor is formed in the p-doped inner area, which partitions the p-doped inner area into two regions one of said regions forming the drain and the other region forming the source of the transistor.

14. The method of Claim 13, wherein a p-doped area having heavier doping that that of the p-doped inner area is inserted in the regions of the p-doped inner area forming the drain and the source, respectively.

15. The method of Claim 13 or 14, wherein an n-doped area having heavier doping than that of the n-doped area forming the gate is inserted into the n-doped area forming the gate.

16. The method of Claim 1, wherein an n-doped area enclosing each active area is produced in the semiconductor substrate for the purpose of separation of active areas for individual semiconductor components.

17. The method of Claim 16, wherein the n-doped area enclosing the active area extends up to the n-doped trough of the semiconductor substrate.

18. The method of Claim 1, wherein for the separation of active areas for individual semiconductor components in the semiconductor substrate prior to ion implantation a mask enclosing each active area is applied to the semiconductor substrate and after application of the mask the n-doped trough is produced in the semiconductor substrate by means of ion implantation, such that the trough is pulled up in the area underlying the mask.

19. The method of Claim 18, wherein an n-doped area that extends up to the raised area of the n-doped trough is produced in the semiconductor substrate.

20. The method of Claim 18, wherein an oxide layer in the semiconductor substrate produces an area of the n-doped trough reaching upward to beneath the oxide.

21. The method of Claim 1, wherein active areas for the individual semiconductor components are separated in the semiconductor substrate by trenches.

22. The method of one of Claims 16 to 21, wherein n-doped or p-doped areas for the creation of the structures forming the semiconductor components are produced in the active areas.

23. The method of Claim 1, wherein for the creation of the structure forming a photosensitive diode at the fringe area of the n-doped trough an initial terminal is created and at the p-doped inner area a second terminal is created.

24. The method of Claim 1, wherein for the creation of the structure forming a photosensitive diode in the semiconductor substrate outside of the n-doped trough a p-doped area is implanted, whereby the first terminal is created at the p-doped area implanted into the semiconductor substrate and the second terminal is created at the fringe area of the n-doped trough.

25. A method for the creation of a structure forming a photosensitive transistor in which an n-doped area is implanted into the p-doped inner area, whereby the terminal forming the collector at the fringe area of the n-doped trough and the terminal forming the emitter at the n-doped area implanted into the p-doped inner area is created.

26. The method of one of Claims 1 to 25, wherein the p-doped or the n-doped semiconductor substrate is a weakly p-doped or n-doped semiconductor substrate.

27. The method of Claim 1, wherein for the creation of a lateral transistor in the n-doped trough or p-doped trough of the semiconductor substrate an n-doped or p-doped trough forming a second diactive base of the transistor is produced by means of ion implantation.

ABSTRACT OF DISCLOSURE

The invention relates to a method for producing integrable semiconductor components, especially transistors or logic gates, using a p-doped semiconductor substrate. First of all, a mask is applied to the semiconductor substrate in order to define a window that is delimited by a peripheral edge. An n-doped trough is then produced in the semiconductor substrate by means of ion implantation using an energy that is sufficient for ensuring that a p-doped inner area remains on the surface of the semiconductor substrate. The edge area of the n-doped trough extends as far as the surface of the semiconductor substrate. The other n-doped and/or p-doped areas that make up the structure of the transistor or logic gate are then inserted into the p-doped inner area of the semiconductor substrate. The inventive method is advantageous in that it no longer comprises expensive epitaxy and insulation processes. In an n-doped semiconductor substrate, all of the implanted ions are replaced by the complementary species; i.e. n is exchanged for p and vice versa.

PCT ARTICLE 19 AMENDMENT

CHANGED PATENT CLAIMS

[Received at the International Bureau on March 13, 2000 (13.03.00); Original Claim 1 changed; all other Claims remain unchanged (1 page)]

1. A method for producing integrable semiconductor components, in particular transistors, diodes, and logic gates, starting with a p-doped or n-doped semiconductor substrate in the following steps:

   application of a mask onto the semiconductor substrate for definition of a window delimited by a peripheral edge;

   production of an n-doped trough in the p-doped semiconductor substrate or p-doped trough in the n-doped semiconductor substrate by means of ion implantation through the mask using an energy that will assure that a p-doped or an n-doped inner area remains on the surface of the semiconductor substrate, whereby the fringe area of the n-doped or p-doped trough extends up to the surface of the semiconductor substrate, and

   production of additional n-doped and/or p-doped areas in the p-doped or n-doped inner area and in the fringe area of the n-doped or the p-doped trough form the structure of the semiconductor component.

2. The method of Claim 1 wherein, for creation of the structure forming an NPN-transistor, a p-doped area having heavier doping than that of the semiconductor substrate together with the p-doped area enclosed by the p-doped inner area forming the base of the transistor and an n-doped area forming the emitter of the transistor

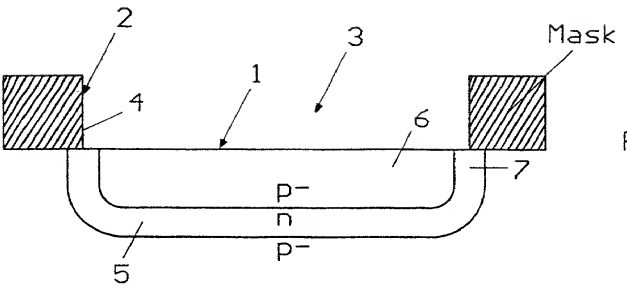

Fig.1a

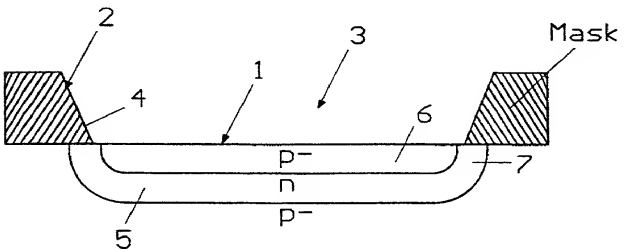

Fig.1b

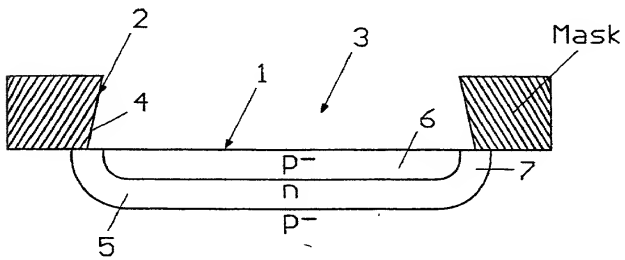

Fig.1c

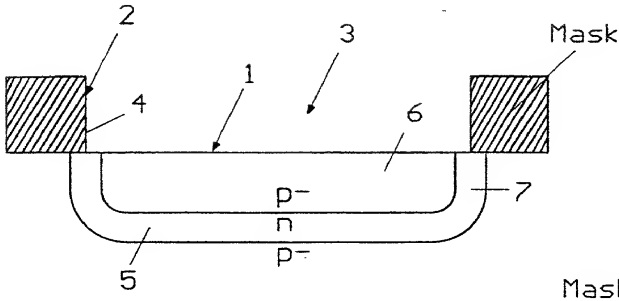

Fig. 2a

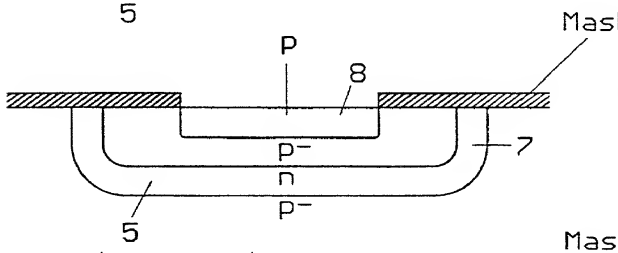

Fig. 2b

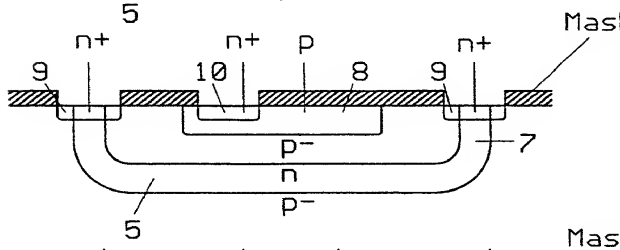

Fig. 2c

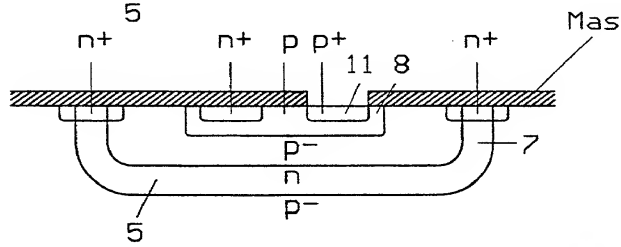

Fig. 2d

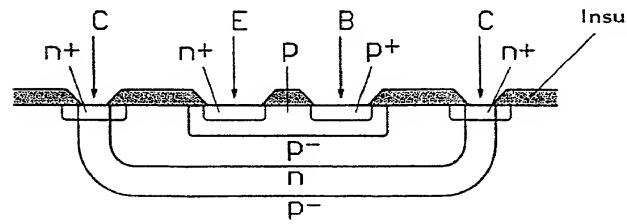

Fig. 2e

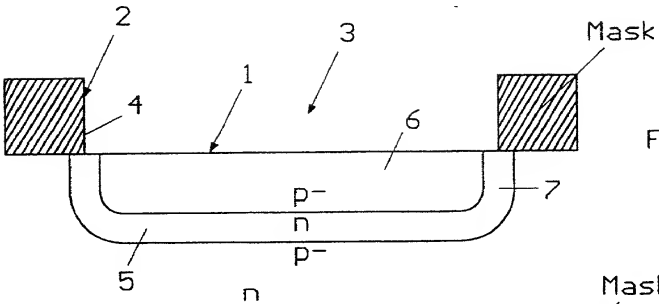

Fig. 3a

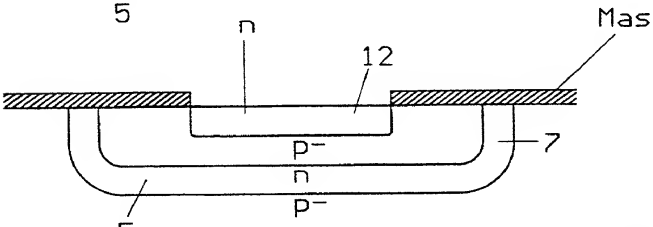

Fig. 3b

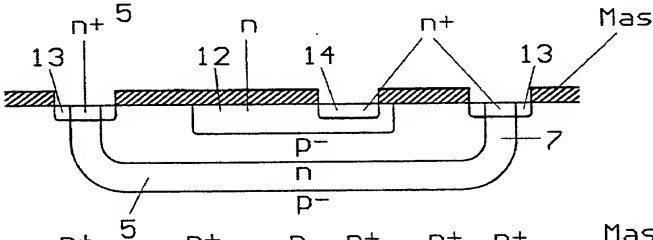

Fig. 3c

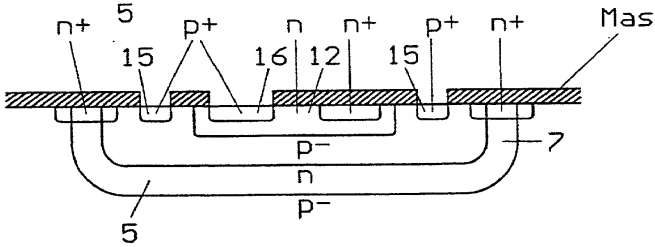

Fig. 3d

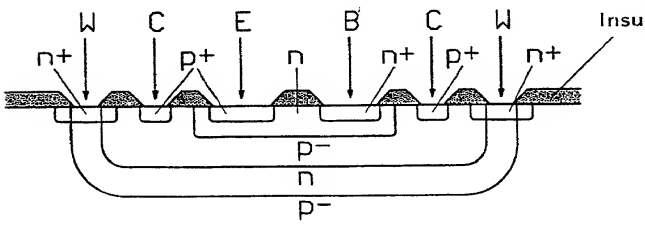

Fig. 3e

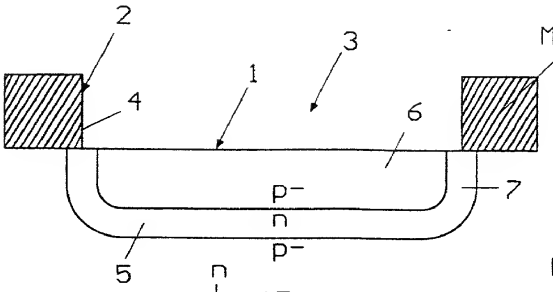

Fig. 4a

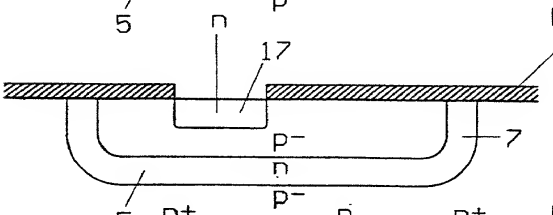

Fig. 4b

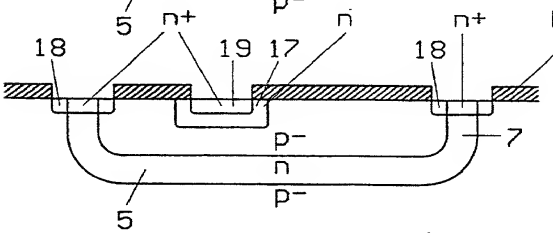

Fig. 4c

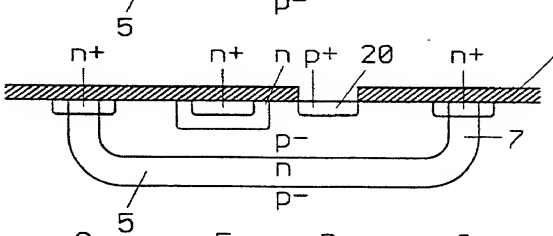

Fig. 4d

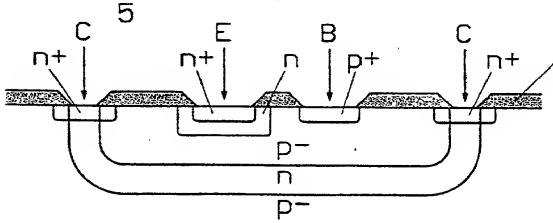

Fig. 4e

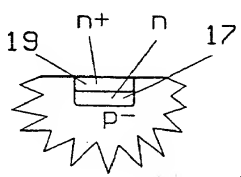

Fig. 4f

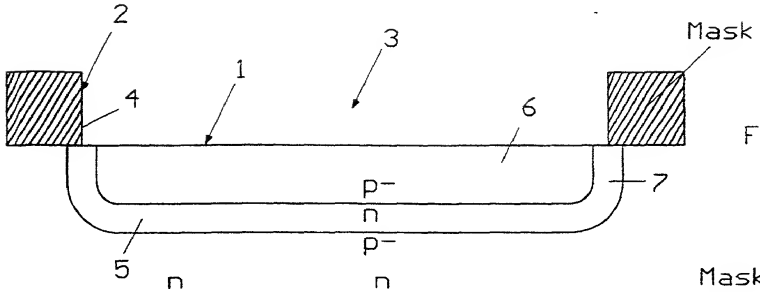

Fig. 5a

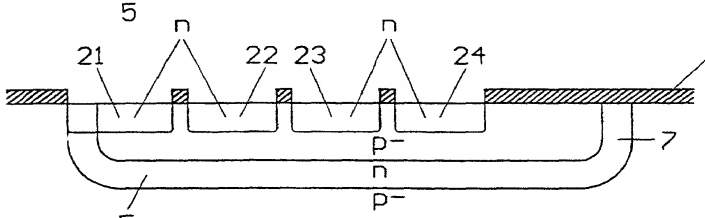

Fig. 5b

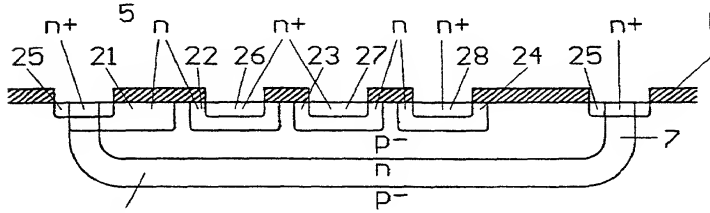

Fig. 5c

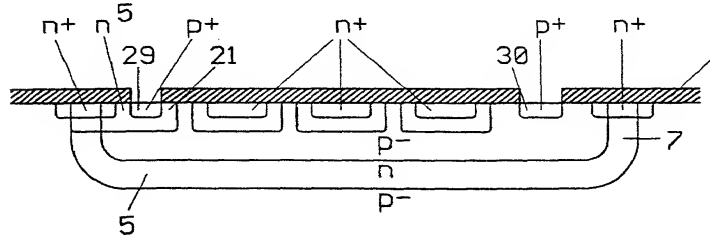

Fig. 5d

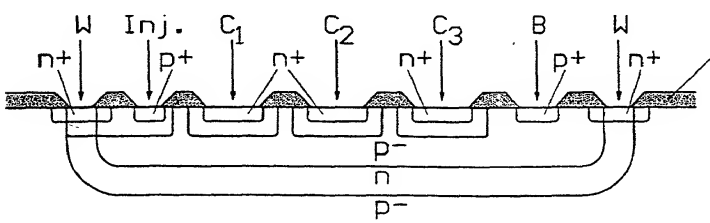

Fig. 5e

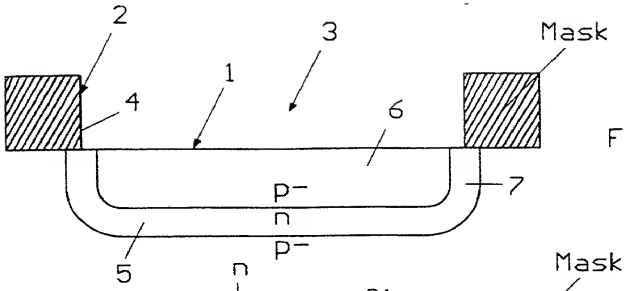

Fig. 6a

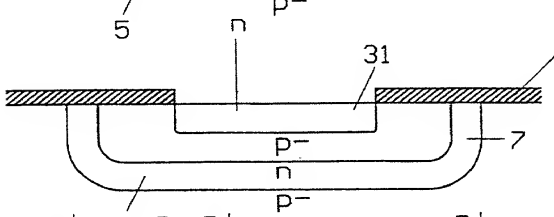

Fig. 6b

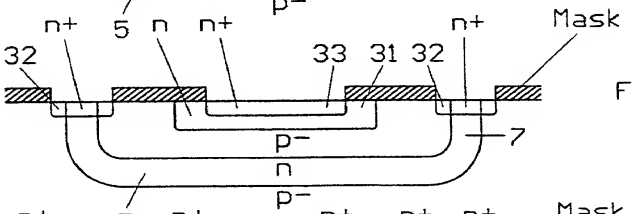

Fig. 6c

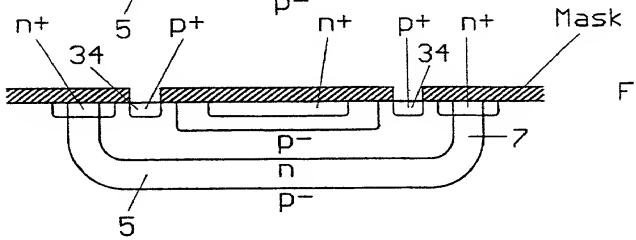

Fig. 6d

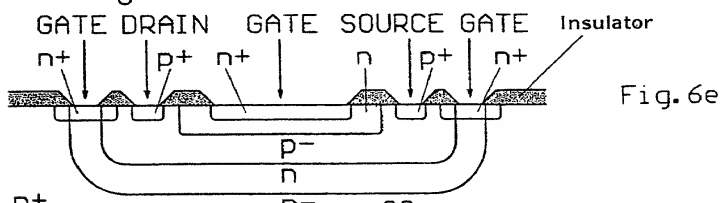

Fig. 6e

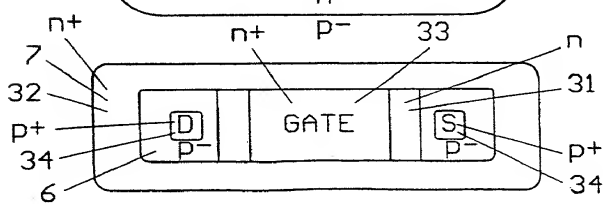

Fig. 6f

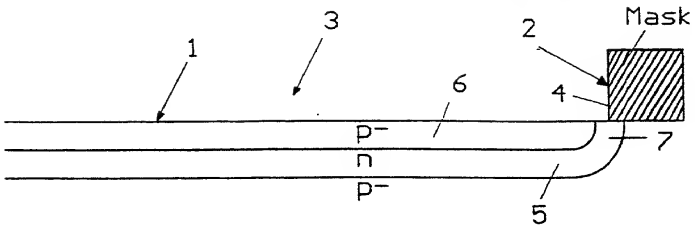

Fig.7a

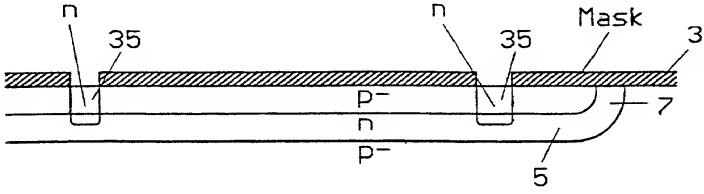

Fig.7b

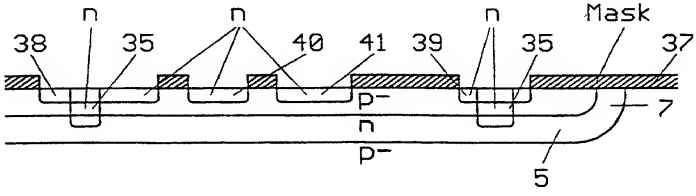

Fig.7c

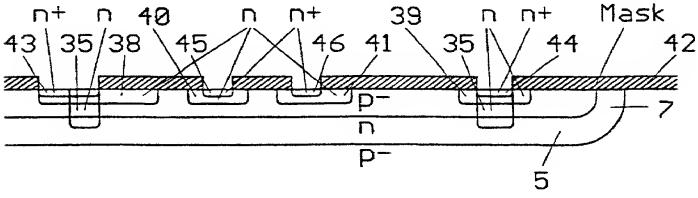

Fig.7d

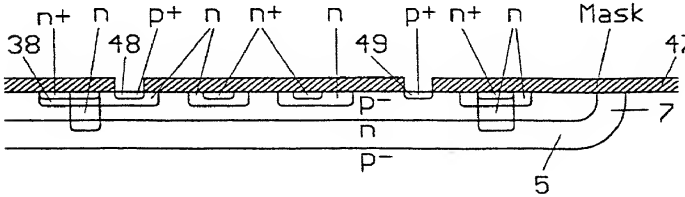

Fig.7e

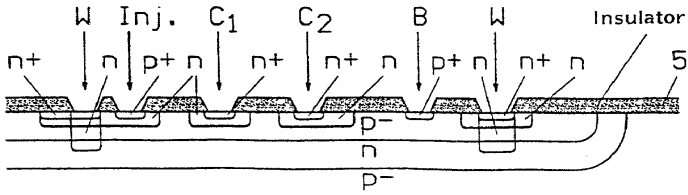

Fig.7f

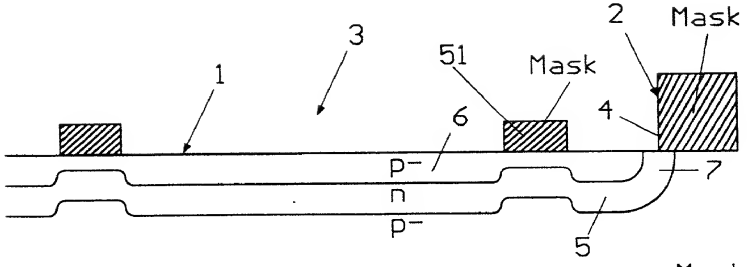

Fig. 8a

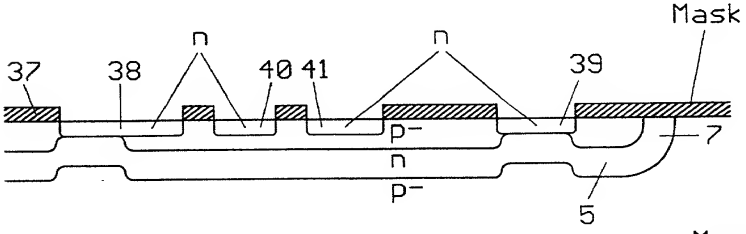

Fig. 8b

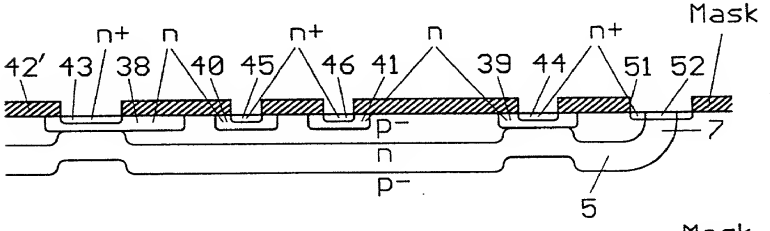

Fig. 8c

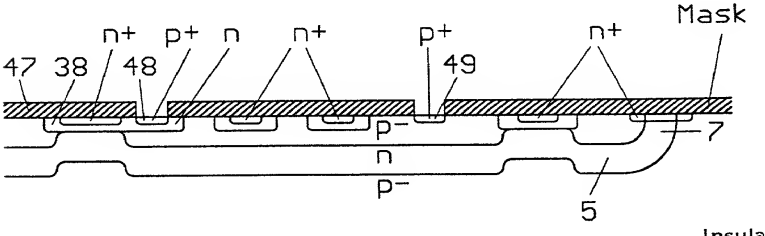

Fig. 8d

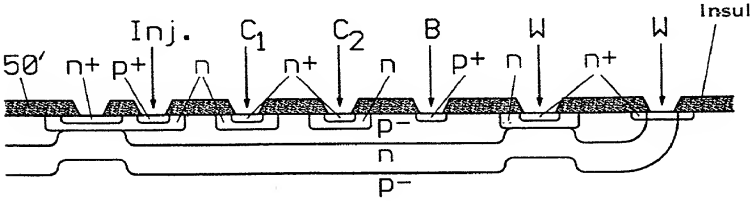

Fig. 8e

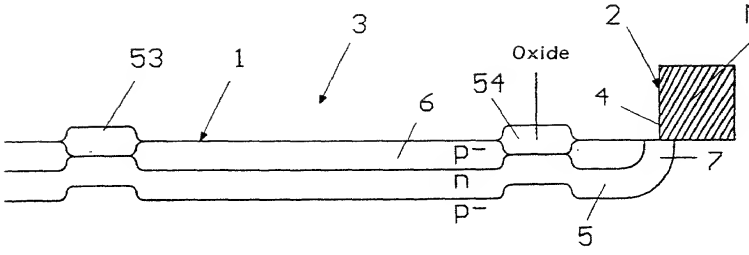

Fig. 9a

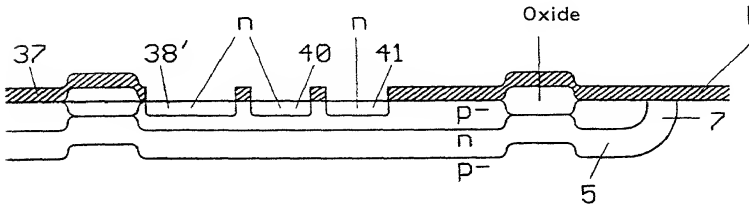

Fig. 9b

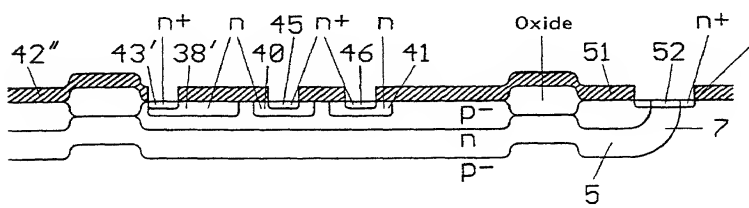

Fig. 9c

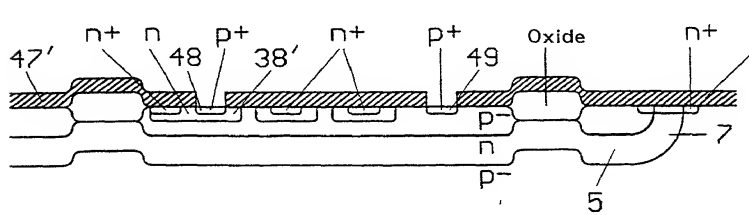

Fig. 9d

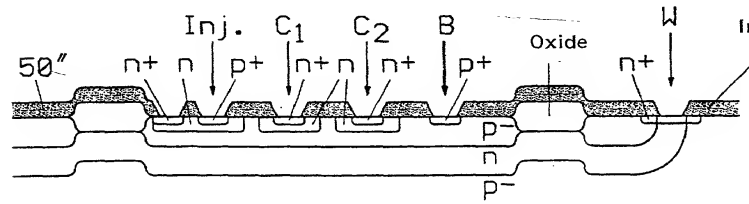

Fig. 9e

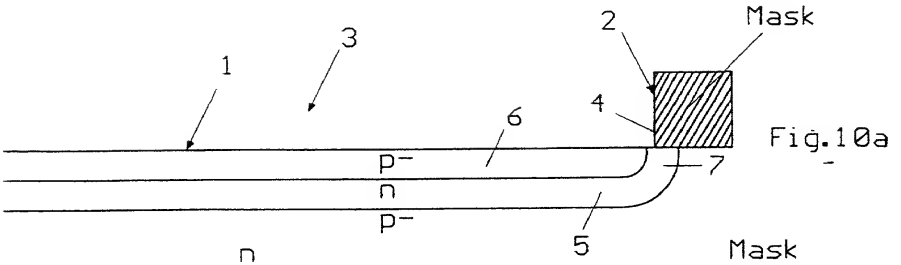

Fig.10a

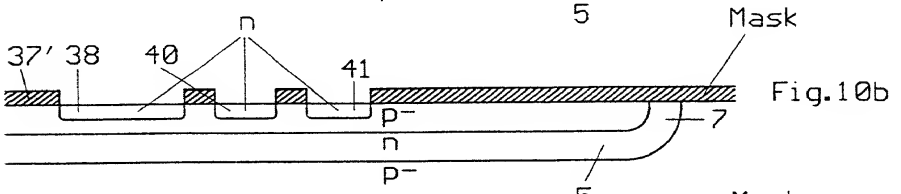

Fig.10b

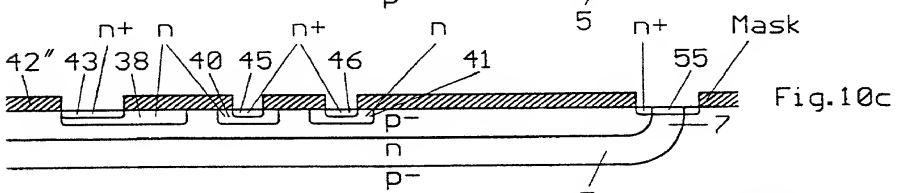

Fig.10c

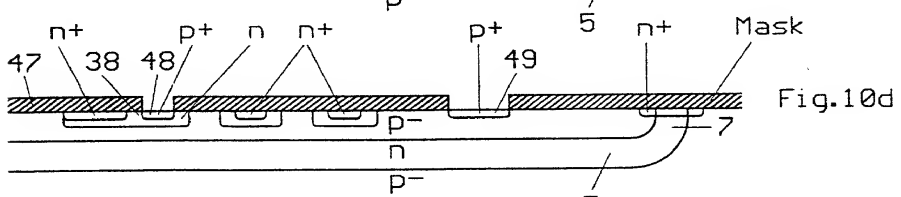

Fig.10d

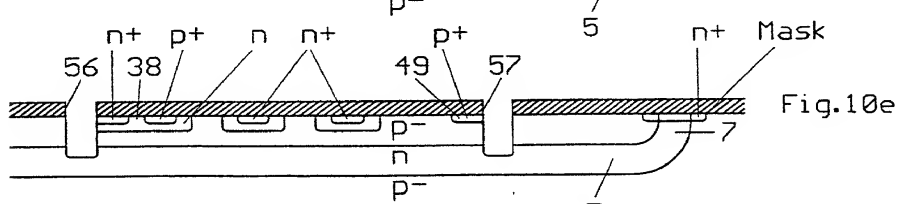

Fig.10e

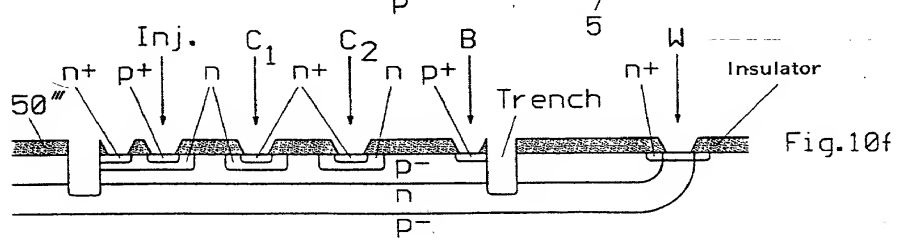

Fig.10f

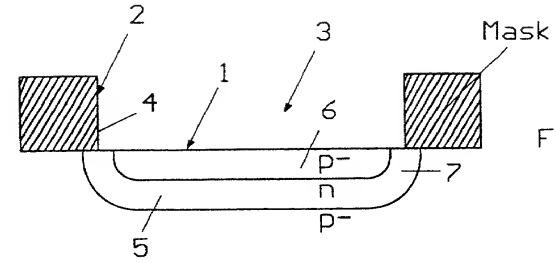

Fig.11a

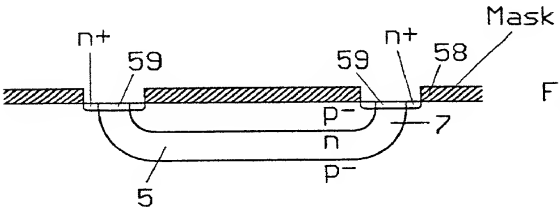

Fig. 11b

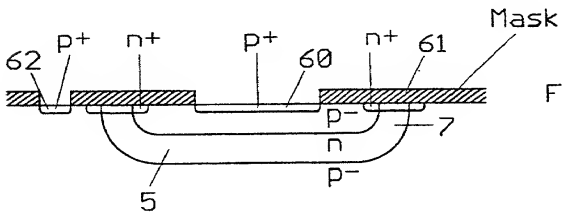

Fig.11c

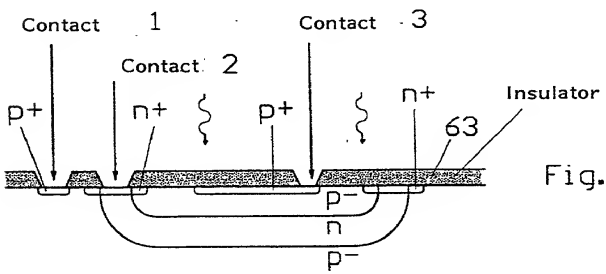

Fig.11d

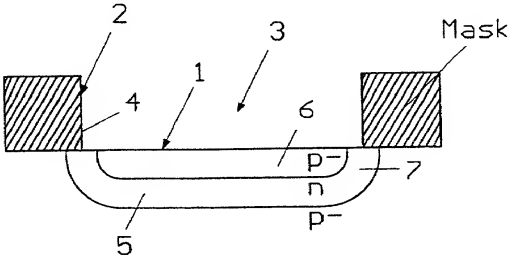

Fig.12a

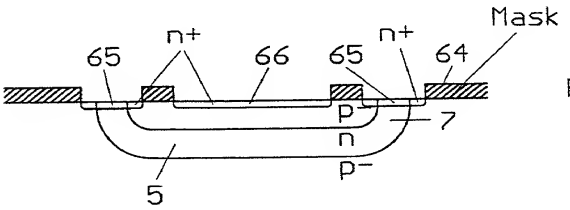

Fig. 12b

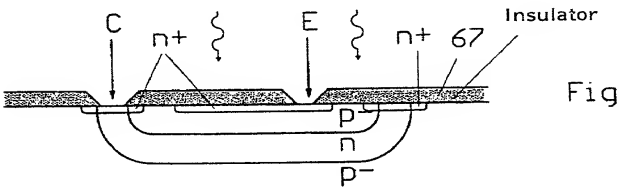

Fig.12c

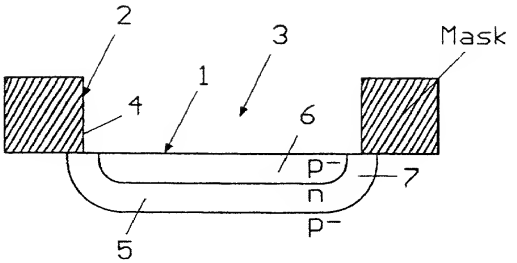

Fig.13a

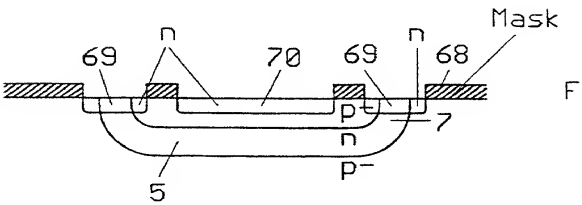

Fig. 13b

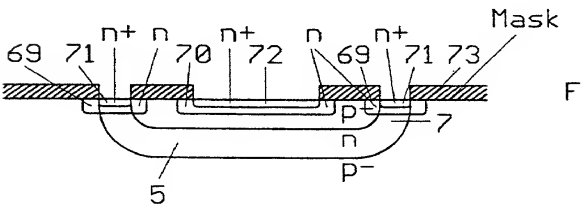

Fig.13c

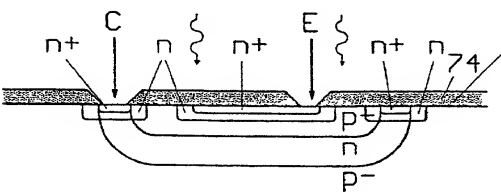

Fig.13d

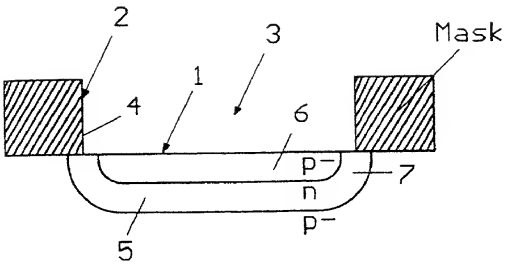

Fig.14a

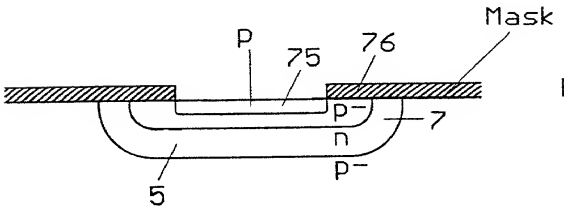

Fig. 14b

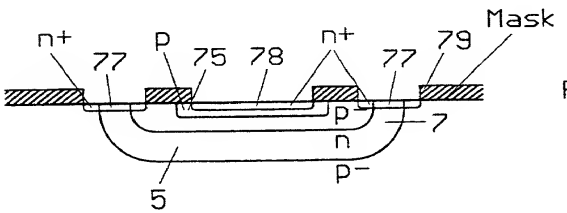

Fig.14c

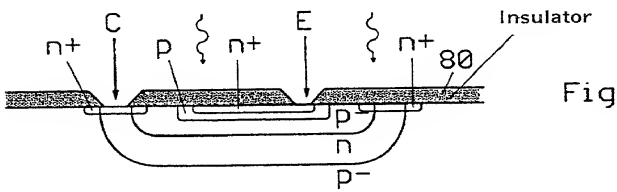

Fig.14d

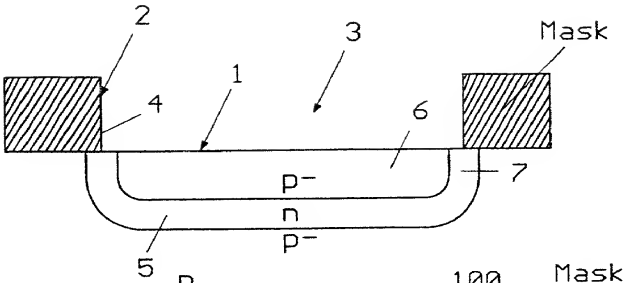

Fig.15a

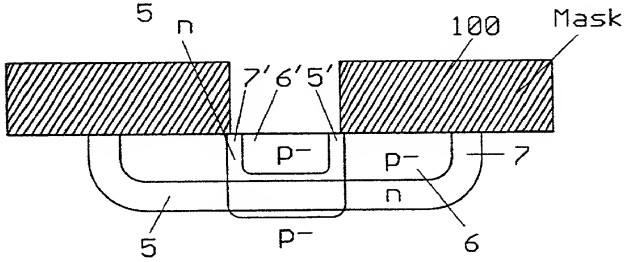

Fig.15b

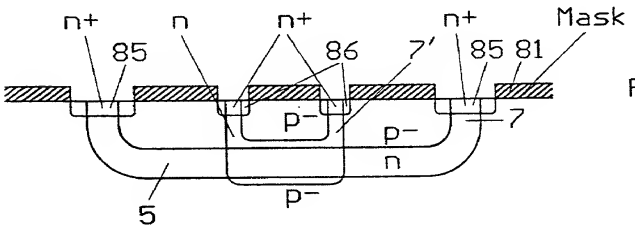

Fig.15c

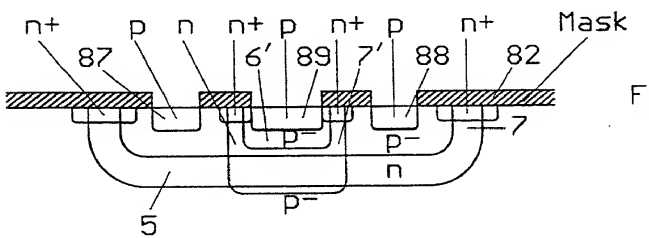

Fig.15d

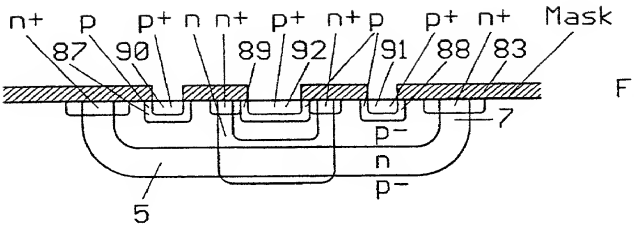

Fig.15e

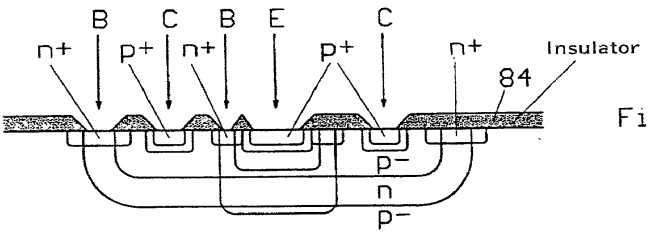

Fig.15f

Docket No.
1477.011

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR PRODUCING TRANSISTORS

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on Aug. 13, 1999 as United States Application No. or PCT International Application Number PCT/EP99/05942

and was amended on March 13, 2000 (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
198 44 531.8 (Number)	Germany (Country)	29/09/98 (Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.) (Filing Date)

(Application Serial No.) (Filing Date)

(Application Serial No.) (Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.) (Filing Date) (Status) (patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status) (patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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